**Amendments to the Claims:**

[1 (c1)] (currently amended)

A system for providing communication between a plurality of cores in an integrated circuit, the system comprising:

a circular segmented bus operatively connected to each of the cores for transferring data between the plurality of cores; and

arbiter means for arbitrating which of the plurality of cores can transmit data at any given time, the arbiter means dynamically segmenting the circular segmented bus to enable plural simultaneous data transmissions on the bus.

[2 (c2)] (original)

The system of claim 1 wherein the circular segmented bus comprises a data bus.

[3 (c3)] (original)

The system of claim 1 wherein the circular segmented bus comprises an address bus.

[4 (c4)] (currently amended)

A system for providing communication between a plurality of cores in an integrated circuit, the system comprising:

a circular segmented bus operatively connected to each of the cores for transferring data between the plurality of cores, ~~The system of claim 1~~ wherein the circular segmented bus comprises a circular bus and isolation means operatively positioned in the circular bus between each pair of adjacent cores; and

arbiter means for arbitrating which of the plurality of cores can transmit data at any given time.

[5 (c5)] (original)

The system of claim 4 wherein the isolation means comprises a plurality of transmission gate switches.

[6 (c6)] (original)

The system of claim 4 wherein the isolation means comprises a plurality of multiplexers.

[7 (c7)] (original)

The system of claim 1 wherein the arbiter means is operatively connected to each of the plurality of cores and receives access requests from the cores.

[8 (c8)] (original)

The system of claim 7 wherein the arbiter means dynamically segments the circular segmented bus responsive to the access requests.

[9 (c9)] (original)

The system of claim 7 wherein the arbiter means dynamically segments the circular segmented bus responsive to the access requests and destinations for data and to provide a maximum number of simultaneous transmissions.

[10 (c10)] (original)

The system of claim 7 wherein the arbiter means dynamically segments the circular segmented bus responsive to the access requests and preselect priorities of the access requests.

[11 (c11)] (original)

An integrated circuit having a reconfigurable bus comprising:

a plurality of cores;

a circular bus;

means for operatively connecting the plurality of cores around the circular bus for transferring data on the circular bus between the plurality of cores;

isolation means operatively positioned in the circular bus between each pair of adjacent cores; and

an arbiter operatively connected to each of the plurality of cores and to the isolation means for arbitrating which of the plurality of cares can transmit data at any given time and reconfiguring the circular bus to isolate segments of the circular bus.

[12 (c12)] (original)

The system of claim 11 wherein the circular bus comprises a data bus.

[13 (c13)] (original)

The system of claim 11 wherein the circular bus comprises an address bus.

[14 (c14)] (original)

The system of claim 11 wherein the isolation means comprises a plurality of transmission gate switches.

[15 (c15)] (original)

The system of claim 11 wherein the isolation means comprises a plurality of multiplexers.

[16 (c16)] (original)

The system of claim 11 wherein the arbiter means receives access requests from the cores.

[17 (c17)] (original)

The system of claim 16 wherein the arbiter means dynamically segments the circular segmented bus responsive to the access requests.

[18 (c18)] (original)

The system of claim 16 wherein the arbiter means dynamically segments the circular segmented bus responsive to the access requests and destinations for data and to provide a maximum number of simultaneous transmissions.

[19 (c19)] (original)

The system of claim 16 wherein the arbiter means dynamically segments the circular segmented bus responsive to the access requests and preselect priorities of the access requests.

[20 (c20)] (original)

The system of claim 11 wherein the plurality of cores comprise bus master circuits and bus slave circuits.

[21 (c21)] (original)

The system of claim 20 wherein the circular bus comprises a split transaction data bus and address bus.

[22 (c22)] (original)

The system of claim 21 wherein one of the bus master circuits is operable to request access to the address bus using a request to the arbiter container more significant address bits in an address operation.

[23 (c23)] (original)

The system of claim 22 wherein a data bus request contains an identification of the one bus master circuit obtained during the address operation.